

The Proper Use of JEDEC Standard Software Data Protection



Application Note

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INTRODUCTION

Single power supply reprogrammable nonvolatile memories, e.g., flash memories, may be unintentionally altered. This occurs because the memory is inadvertently issued a valid Write command. Older reprogrammable nonvolatile memories have a separate high voltage power supply that controls the Write operation making unintentional writes nearly impossible once the high voltage is removed. Since a single power supply flash memory uses the same power supply for reading and writing, externally removing the high voltage supply is not available. Therefore, alternate means of avoiding inadvertent writes is required.

For reprogrammable nonvolatile memories, various control signals are used to control the state of the memory, e.g., read, write, or standby. The data in a Page-Mode flash memory is altered by writing a page. The data is loaded into an on-chip buffer, then an internally controlled write cycle alters the contents of the page. The inadvertent or false write happens when the memory control signals deviated from the desired read or standby state due to noise. The noise occurs on the power supply line, the ground line, the control lines, or in some combination. The noise is often worse during power-up or power-down.

The industry has developed several means to provide inadvertent write protections. These include:

1. Inhibiting the write until the power supply is within the specified range
2. Using multiple control lines that must be at different levels to initiate a write
3. Using a filter on the control lines to eliminate transient high frequency noise

All of these methods have been proven ineffective in some systems.

The most effective means of preventing inadvertent write is use of the JEDEC standard Software Data Protection (SDP) method.

The SDP method is the use of a specific 3-byte sequence in order to enter the Write mode. Since this specific combination of addresses, data, and control signals is virtually impossible to unintentionally generate, the device is protected from all inadvertent write commands. The SDP Enable command consists of the 3-byte sequence. This enables SDP protection without altering memory contents. The SDP Write command is the same 3-byte sequence as the normal Page-Write. The SDP Write command is used to intentionally alter memory contents after SDP has been enabled.

3-BYTE COMMAND SEQUENCE

With SDP enabled, no write can occur unless preceded by a specific 3-byte command sequence. The 3-byte SDP command sequences are immune to noise, therefore, inadvertent writes are prevented. The 3-byte SDP Enable command sequence that enables SDP is the same 3-byte Write command sequence that allows a valid write to occur after SDP is enabled.

SDP must always be enabled when using single power supply flash memories.

With SDP enabled, the 3-byte SDP Write command sequence is used to write a page of data to the memory. This prevents any unintentional alteration of memory contents due to a false write.

SDP MUST BE ENABLED

Historically, primitive programmers could not write memories using the SDP command sequence. Therefore, many reprogrammable nonvolatile single power supply memories have SDP as an option. These memories are shipped with SDP disabled so that the primitive programmers can write the memory.

SST strongly recommends, that after using one of these programmers and installation of the memory into the user's system, the first system write to the memory uses the 3-byte SDP Write command sequence making SDP protection continuous.

However, most programmers now have the capability to utilize the 3-byte SDP Write command sequence; therefore, SST strongly recommends the memory be written using the 3-byte SDP Write command sequence. Each page of the memory is written using the 3-byte SDP Write command sequence. Therefore, the memory is protected while writing in the programmer and SDP is already enabled when the memory is installed in the user's system.

Some programmers cannot write using SDP, but have the capability of enabling SDP after the memory is written. This capability is often called "security" and is an option that must be enabled by the programmer operator. SST strongly recommends that when using this type of programmer the "security" option is always enabled, i.e., the SDP Enable command is issued by the programmer after the completion of writing the memory. Thus, SDP is already enabled when the memory is installed in the user's system.



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Note, the SDP Enable command and the SDP Write command use the same 3-byte sequence. Thus, in the system, separate SDP enable and SDP Write command sequences are not required. Using the 3-byte SDP Write command every time the device is to be written, will assure maximum protection.

Since, on many memories, SDP is an option that can be enabled, there is also a disable command. SDP is disabled by issuing a 6-byte SDP Disable command sequence. The disable command sequence has sometimes to be used with programmers that do not have the capability of writing the memory with SDP enabled. As described above, if SDP is disabled when using this type of programmer, then SDP should be enabled, i.e., "security" set, as the final step in the programmer operation. Thus, SDP will be enabled when the memory is installed in the user's system.

Some system applications have used the 6-byte SDP Disable command sequence prior to writing large blocks, e.g., many pages, of the memory. The idea is to save system overhead by not having to issue the 3-byte SDP Write command sequence prior to writing each page. However, the overhead in using SDP is small compared with the total time to write the memory; thus, there is very little real time savings. Since the security factor of SDP far outweighs the negligible time savings, the SDP should never be disabled in the user's system.

SUMMARY

In summary, for proper operation of SST single power supply Page-Mode flash memories, the following guidelines are strongly recommended:

1. SDP must always be enabled in order to avoid inadvertent writes.
2. The 3-byte SDP Write command sequence must always be issued, whenever performing a write. Please refer the "Enable Software Data Protection Page-Write" timing diagram in the applicable SST data sheet.
3. The 6-byte command sequence to disable SDP should never be issued.

SDP is an important JEDEC standard for use with single power supply flash memories to provide data security. To achieve the maximum system benefit, SDP must always be enabled and writing must always be performed using the 3-byte SDP Write command sequence.