

FlashFlex51 Microcontroller Oscillator Circuit Design Considerations



Application Note

June 2003

1.0 INTRODUCTION

The SST FlashFlex51 family of microcontrollers has two modes of clock operation: on-chip oscillator and external clock drive. This application note provides oscillator circuit design considerations for the on-chip oscillator mode.

2.0 ON-CHIP OSCILLATOR

XTAL1 and XTAL2 are the input and output of an inverting amplifier as shown in Figure 5-1 below. The internal feedback resistor, R_f , biases the inverter in its linear region and forms a closed loop feedback system. A quartz crystal along with a pair of loading capacitors makes up the external portion of the oscillator circuit. An optional series resistor, R_s , may be used to limit the overall gain if the crystal is being overdriven.

3.0 EXTERNAL COMPONENTS SELECTION

Crystal manufacturer, supply voltage, and other factors may cause circuit performance to differ from one application to another. C1 and C2 should be adjusted appropriately for each design. Table 3-1 suggests some typical values for C1 and C2 versus crystal type for various frequencies. If the circuit is being overdriven following the satisfactory selection of all external components, a series resistor, R_s , should be added. If there is voltage clipping between V_{DD} and V_{SS} , that is usually a good indication that the crystal is being overdriven. An R_s value of 100-200 Ω is recommended.

TABLE 3-1: RECOMMENDED VALUES FOR C1 AND C2 BY CRYSTAL TYPE

Crystal	C1 = C2
Quartz	20-30pF
Ceramic	40-50pF

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4.0 AMPLIFIER GAIN

The oscillator circuit consists of an amplifier and a feedback network. In order for oscillation to commence, two conditions must be met: 1) the overall loop gain must be equal to unity. 2) The phase shift must be 0° or 360°. The loading capacitors C1 and C2 must be properly selected to ensure these above conditions are met.

5.0 STABILITY

Stability is achieved once the oscillator is resonant at the desired frequency. Various parameters affect frequency stability but not all are critical. Some parameters a designer should consider are: Temperature, drive level, crystal aging, crystal tolerance and deviation over temperature and frictional wear. Increasing C1 and C2 will improve frequency stability by limiting the drive level, but that also increases startup time. Instead of increasing C1 and C2, use a series resistor, R_s , to reduce the drive level.

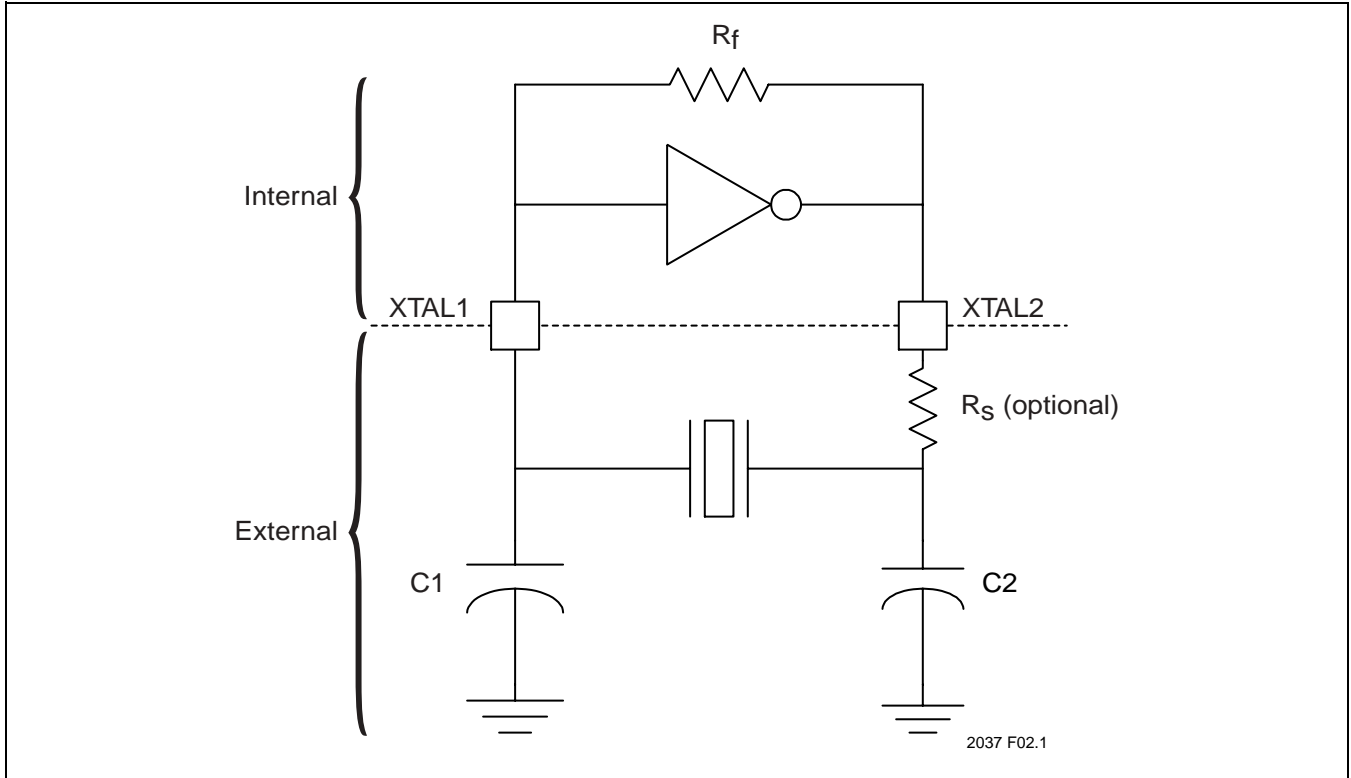


FIGURE 5-1: ON-CHIP OSCILLATOR

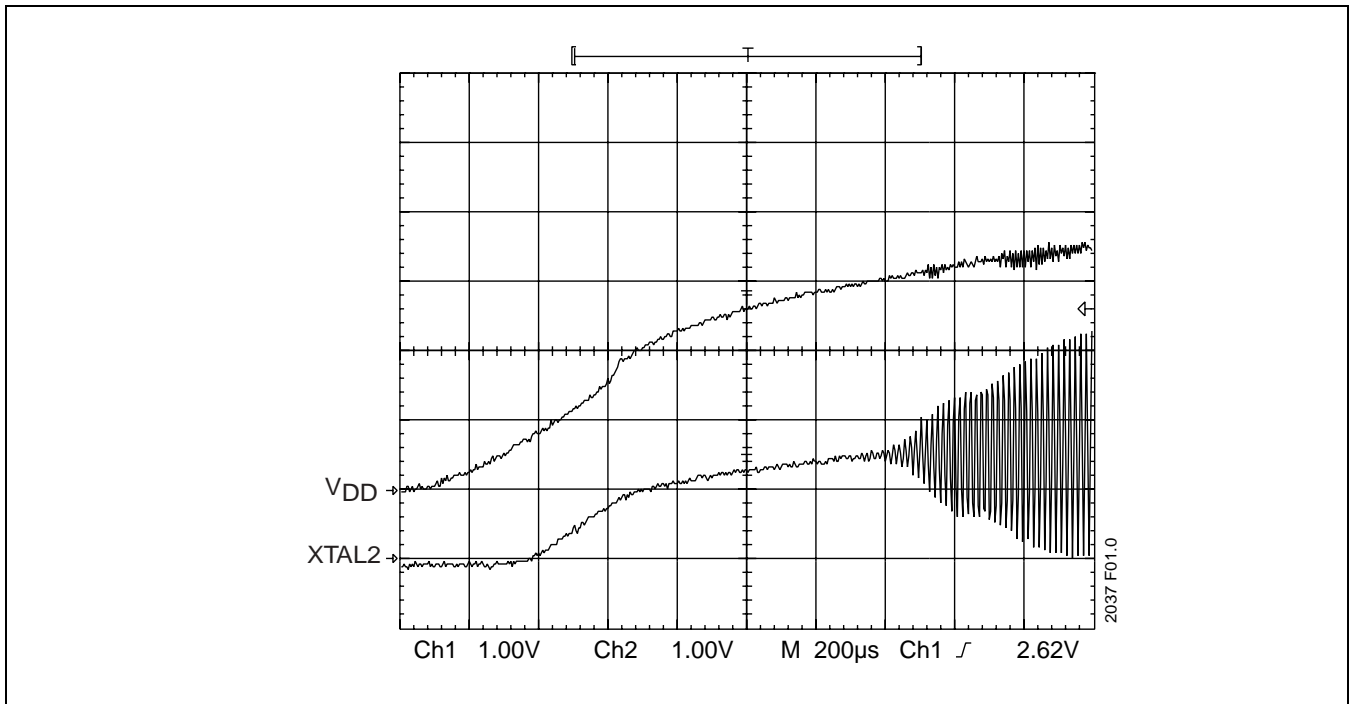


FIGURE 5-2: OSCILLATOR STARTUP FOR A 11.0592 MHz CRYSTAL

6.0 THIRD OVERTONE CRYSTALS

At operating frequencies above 25 MHz, fundamental mode quartz crystals become expensive or very difficult to obtain. Thus nearly all readily available quartz crystals in the 25 MHz to 40 MHz range are of the third overtone variety. However, without additional circuit modifications, the crystal circuit will continue to oscillate at a fundamental mode frequency that is approximately one-third the overtone frequency.

One way of attaining overtone mode operation is via a LC tank circuit at the output of the oscillator circuit that dampens the fundamental mode frequency and accentuates the overtone mode frequency. Such a circuit is shown in Figure

6-1 where C2 and L3 form a resonant circuit at the desired overtone frequency. In this circuit, C3 is a de-coupling capacitor used so that the DC bias voltage is not affected. Acceptable values are in the range of 1 nF to 10 nF. The value of the inductor L3 may be obtained using the following equation:

$$L_3 = 1/((2\pi \times f)^2 \times C_2), \text{ f = desired frequency}$$

However these value are not highly critical due to the wide bandwidth of the filter and a typical inductor value of 1.5 μ H and a capacitor C3 value of 4.7 nF should be acceptable for a wide range of frequencies.

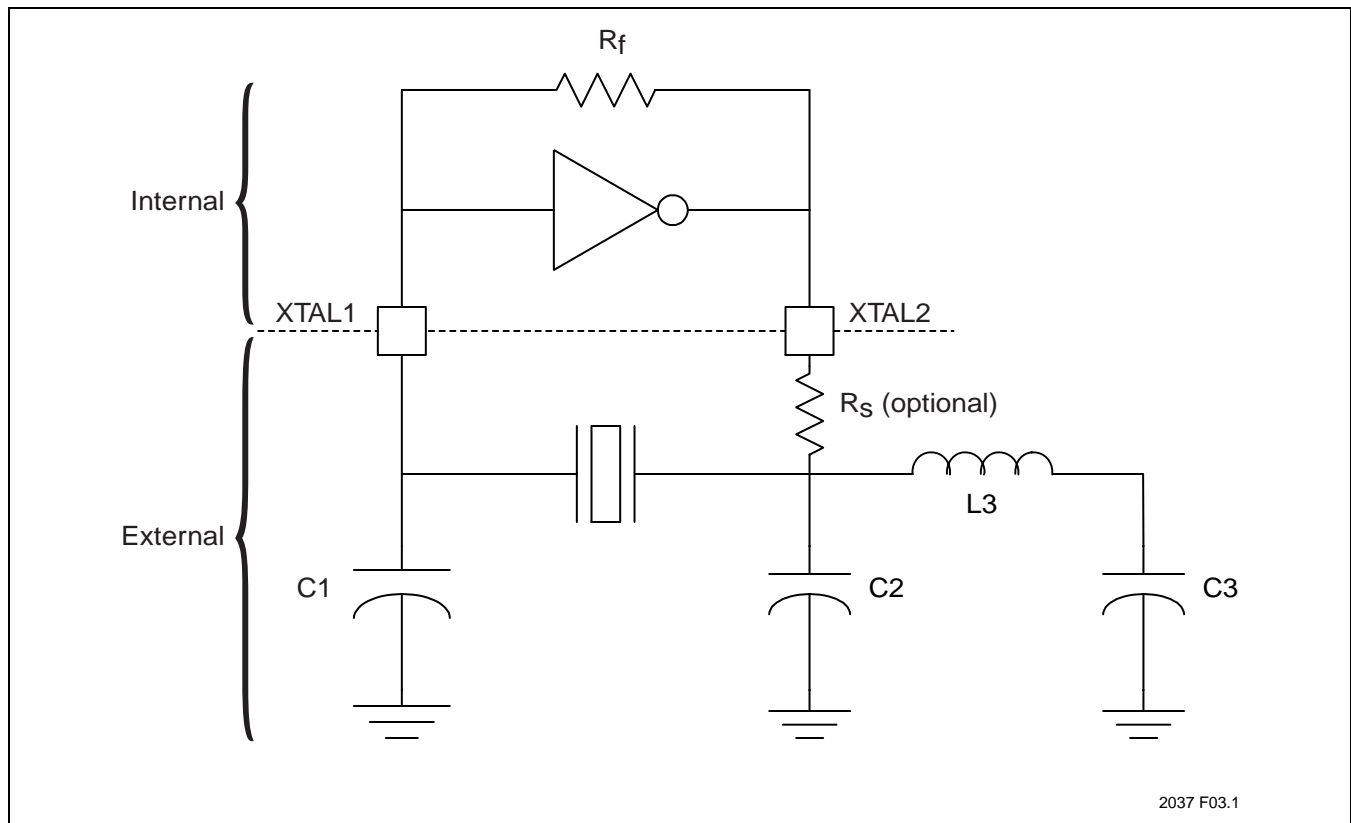


FIGURE 6-1: OVERTONE CRYSTAL OSCILLATOR CIRCUIT



7.0 DOUBLE-CLOCK MODE

Some devices in the FlashFlex51 microcontroller family support a feature that will internally double the operating frequency. With this option, it would be possible to use fundamental mode quartz crystals under 25 MHz to attain internal operating frequencies up to 40 MHz. When double-clock mode is enabled, all internal operations run at twice the speed except the watchdog timer. Once double-clock mode is enabled, it will remain in effect until the chip is erased. Review the device data sheet to determine if this feature is supported.

There are three ways to enable double-clock mode. The first method is using a universal programmer that supports the FlashFlex51 microcontroller family. A second method is to use the EasyIAP PC software with a FlashFlex51 device that has the SST bootstrap loader (BSL) installed on it. This software and associated documentation may be obtained from the SST website.

The last method to enable double-clock mode is through In-Application Programming (IAP) which allows flash reprogramming while executing code. Please review the SST application note, *FlashFlex51 Microcontroller In-Application Programming Basics*, to learn how IAP mode operates. The following sample code demonstrates how to enable double-clock mode using IAP. One restriction with this technique is that the code must be executed from block 1 or external code memory.

```
ORL    SFCF, #040h    ; enable IAP
MOV    SFAH, #055h
MOV    SFAL, #000h
MOV    SFDT, #0AAh
MOV    SFCM, #08h    ; clock-double command
WAIT:  MOV    A, SFST    ; check IAP status
        JB     ACC.2, WAIT ; wait till done
        ANL   SFCF, #0BFh ; disable IAP
```

Lastly, it is possible to query in software if the double-clock mode is enabled by examining SFR bit SFST[3]. When double-clock mode is enabled, SFST[3] is set to 1.

8.0 STARTUP TIME

Startup time is critical in an oscillator circuit because of the microcontroller's reset and initialization requirements. Most crystal oscillator circuits typically take between 0.5 ms to 20 ms to start up. Figure 5-2 shows the startup time for an 11.0592 MHz crystal oscillator circuit. For a low frequency crystal, the startup may take up to several seconds. The latency in startup time can disrupt the Power-on Reset process. To ensure a proper reset, the oscillator must be stable for at least two machine cycles (24 clocks) after achieving stable resonance. Therefore, for a low frequency crystal, it is necessary to extend the reset signal to avoid an invalid reset.

The loading capacitors C1 and C2 should be kept small to minimize startup time, but robust enough to provide adequate gain for startup. A higher C2 value can increase the phase shift across the crystal at power-up and help increase the startup time.

9.0 PCB DESIGN

Certain design guidelines must be followed for a good oscillator circuit. Stray capacitances and large inductances must be kept to a minimum to avoid an undesired mode of oscillation and startup issues. A good practice is to keep all trace lengths as short as possible. Components should be isolated in order to prevent signal coupling. Ground planes should be used to isolate signals. Special precautions must be taken for single or double layer board designs with no ground planes. Additionally, a 0.1µF ceramic high frequency, low inductance capacitor connected between VDD and Ground should be placed as close to the package terminals as possible to remove power line noise. Refer to the application note, *FlashFlex51 Microcontroller PCB Design Considerations*, for general PCB design guidelines.