

# Migration from SST28SF040A to SST29SF040



*Application Note*  
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## INTRODUCTION

The SST29SF040 is a newer Small-Sector flash product compared with the SST28SF040A. All SST28SF040A users are encouraged to migrate to SST29SF040 due to its higher performance.

## HARDWARE COMPARISON

### Advantages of the SST29SF040

- **Smaller TSOP package**

The SST29SF040 is offered in an 8mmx14mm, 32-TSOP package while the SST28SF040A is offered in an 8mmx20mm 32-TSOP package.

The smaller package saves valuable space on the PCB.
- **Smaller sector size**

The SST29SF040 offers a uniform sector size of 128 bytes, half that of the SST28SF040A, which allows more flexible and efficient use of memory space.
- **Lower active power consumption**

In active mode, current consumed by the SST29SF040 is 10mA (typical) compared to the SST28SF040A which is 15mA (typical).
- **Shorter read access time**

Typical read access time is 55ns for SST29SF040 and 90/120ns for SST28SF040A.
- **Faster Byte-Program speed**

Byte-Program can be completed within 14µs in SST29SF040 and 35µs in SST28SF040A.
- **Faster chip rewrite speed**

Chip rewrite time is 8 sec for SST29SF040 compared to 20 sec for the SST28SF040A

## Hardware Design Modifications

### 32-TSOP Packages

Both the SST29SF040 and the SST28SF040A are offered in 32-lead TSOP packages, with sizes of 8mmx14mm and 8mmx20mm respectively.

Existing designs utilizing the larger SST28SF040A require only a minor hardware change. Simply extending the traces will allow customers to migrate to the smaller SST29SF040 TSOP package.

### 32-PDIP Packages

Customers wanting to migrate from the SST28SF040A PDIP package to the SST29SF040 in either the PLCC or TSOP packages will need to redesign the PCB layout.

### 32-PLCC Packages

Customers currently using the SST28SF040A PLCC package can migrate to the SST29SF040 without any hardware changes.

## SOFTWARE COMPARISON

### Required Software Modifications

The SST29SF040 provides the JEDEC approved Software Data Protection scheme for all data alteration operations. The SST28SF040A requires a 2-step command sequence scheme for data alteration and 7 read-cycle sequence scheme for software data protect/unprotect. These completely different command sequence schemes make software modification mandatory.

The command sequences of the SST28SF040A and the SST29SF040 are shown in Table 1 and Table 2. Any command used for the SST28SF040A should be replaced by its counterpart for the SST29SF040 in application code.



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**TABLE 1: SOFTWARE COMMAND SUMMARY FOR THE SST28SF040A**

Command Summary	Required Cycle(s)	Setup Command Cycle			Execute Command Cycle			SDP <sup>5</sup>
		Type <sup>1</sup>	Addr <sup>2,3</sup>	Data <sup>4</sup>	Type <sup>1</sup>	Addr <sup>2,3</sup>	Data <sup>4</sup>	
Byte-Program	2	W	X	10H	W	PA	PD	N
Sector-Erase	2	W	X	20H	W	SA	D0H	N
Chip-Erase <sup>6</sup>	2	W	X	30H	W	X	30H	N
Reset	1	W	X	FFH				Y
Read-ID	2	W	X	90H	R	7	7	Y
Software Data Protect	7	R	8					
Software Data Unprotect	7	R	9					

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1. Type definition: W = Write, R = Read, X can be V<sub>IL</sub> or V<sub>IH</sub>, but no other value.
2. Addr (Address) definition: SA = Sector Address = A<sub>18</sub>-A<sub>8</sub>, sector size = 256 Bytes; A<sub>7</sub>-A<sub>0</sub> = X for this command.
3. Addr (Address) definition: PA = Program Address = A<sub>18</sub>-A<sub>0</sub>.
4. Data definition: PD = Program Data, H = number in hex.
5. SDP = Software Data Protect mode using 7 Read Cycle Sequence.
  - a) Y = the operation can be executed with protection enabled
  - b) N = the operation cannot be executed with protection enabled
6. The Chip-Erase function is not supported on industrial temperature parts.
7. Address 0000H retrieves the Manufacturer's ID of BFH and address 0001H retrieves the Device ID of 04H.
8. Refer to Figure 11 in the data sheet for the 7 Read Cycle sequence for Software-Data-Protect.
9. Refer to Figure 10 in the data sheet for the 7 Read Cycle sequence for Software-Data-Unprotect.

**TABLE 2: SOFTWARE COMMAND SEQUENCE FOR THE SST29SF040**

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data	Addr <sup>1</sup>	Data
Byte-Program	555H	AAH	2AAH	55H	555H	A0H	BA <sup>2</sup>	Data				
Sector-Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA <sub>X</sub> <sup>3</sup>	20H
Chip-Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Software ID Entry <sup>4,5</sup>	555H	AAH	2AAH	55H	555H	90H						
Software ID Exit <sup>6</sup>	XXH	F0H										
Software ID Exit <sup>6</sup>	555H	AAH	2AAH	55H	555H	F0H						

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1. Address format A<sub>14</sub>-A<sub>0</sub> (Hex),  
 Addresses A<sub>MS</sub>-A<sub>15</sub> can be V<sub>IL</sub> or V<sub>IH</sub>, but no other value, for the Command sequence for SST29SF040.  
 A<sub>MS</sub> = Most significant address  
 A<sub>MS</sub> = A<sub>18</sub> for SST29SF040.
2. BA = Program Byte address
3. SA<sub>X</sub> for Sector-Erase; uses A<sub>MS</sub>-A<sub>7</sub> address lines for SST29SF040
4. The device does not remain in Software Product ID mode if powered down.
5. With A<sub>MS</sub>-A<sub>1</sub> = 0; SST Manufacturer's ID = BFH, is read with A<sub>0</sub> = 0,  
 SST29SF040 Device ID = 13H, is read with A<sub>0</sub> = 1
6. Both Software ID Exit operations are equivalent

For timing diagrams and other detailed information, please refer to the data sheets for SST28SF040A and SST29SF040 on SST.com