

INTRODUCTION

Endurance is the cumulative number of Erase/Program cycles before the device fails a data sheet parameter. Reprogrammable nonvolatile memories, such as flash EEPROMs, have a failure rate associated with endurance that is best represented by the classical “bathtub curve.” There are the “infant mortality,” “useful life,” and “wear-out” regions. When attempting to describe the endurance of a device, manufacturers typically claim some number of cycles. In terms of the classical “bathtub” curve, this level is the cumulative number of cycles through the “useful life” region where the cumulative failures are less than a guaranteed value, e.g., 1% for 10,000 cycles. The number of cycles is supposed to be less than the value at the knee of the curve separating the “useful life” region from the “wear-out” region. In practice, the stated level should be significantly less than the actual value at the onset of wear-out. During the “useful life” region, there will be a small, but constant failure rate. The issue facing manufacturers is to assure each device has been screened to eliminate “infant mortality,” has an endurance value greater than the stated level, and the failure rate in the “useful life” region meets industry standards, reference IEEE Std 1005-1998 *Definition and Characterization of Floating Gate Semiconductor Arrays* and JEDEC Test Method A117 for additional information.

FAILURE MECHANISMS

There is lot-to-lot and within-lot variability for endurance failure mechanisms; thus, determination of the individual device endurance value is desirable. Devices can fail during Erase/Program cycling for a variety of failure mechanisms. In general, the causes for these mechanisms can be grouped into four major categories:

Initial defects

Physical anomalies that cause the device to fail during initial testing or “infant mortality” screening; generally caused by wafer processing defects.

Latent defects

Physical anomalies that cause the device to fail after some period of operation; generally caused by wafer processing defects.

Generated defects

Physical anomalies that cause the device to fail after some period of operation, e.g., data retention failures, generally caused by operation of the device, e.g., the TDDB (Time-Dependent-Dielectric-Breakdown) characteristics of charge transfer oxides and the imposed electric fields for erasing or programming.

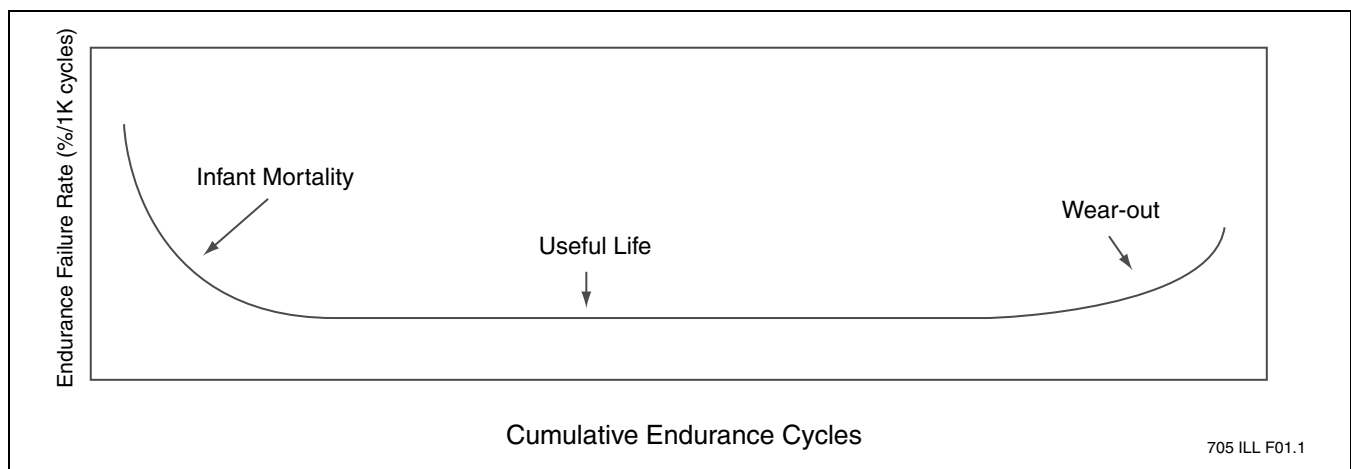


FIGURE 1: CLASSICAL “BATHTUB” CURVE FOR ENDURANCE



Uniform degradation

A steady decline in the performance of a given characteristic that causes the device to fail after some period of operation; generally caused by the deterioration in some physical structure, e.g., from charge trapping.

Initial defects determine the duration and failure rate in the “infant mortality” region. Latent defects establish the failure rate in the “useful life” region. Generated defects and uniform degradation determine the onset of the “wear-out” region. Latent and generated defects are random events that are difficult to measure and predict, so that specific devices with different intrinsic endurance values are difficult to identify. Uniform degradation is strongly correlated with explicit memory cell performance characteristics; thus, specific device endurance can be predicted from measurements of each memory cell in the array, and devices can be segregated by endurance values.

The relative frequency of the 4 categories is technology dependent. For example the thin oxide approaches used by stacked gate and two transistor manufacturers are most susceptible to latent and generated defects, while the thick oxide approach used by SST is most susceptible to uniform degradation. See Table 1.

This means the thin oxide manufacturers have significantly more variation in device-to-device endurance performance and significantly more risk in producing devices or lots with

unacceptable endurance values. SST’s SuperFlash technology provides the ability to accurately predict endurance on a device by device basis; thus, segregate devices by desired endurance levels.

SST TESTING

SST includes Erase/Program cycling, high voltage and high temperature stressing during the test flow to eliminate the “infant mortality” failures. Latent and generated defects are minimized by the use of thick oxides, in addition to normal wafer fabrication cleanliness and statistical process control. Additionally, due to the patented unique nature of the SST memory cell, SST includes test routines to compare each memory cell’s performance to empirically generated criteria to verify the device meets SST specifications for uniform degradation. This assures each SST lot meets the guaranteed endurance level. The process is very similar to the separation of devices into various speed grades, i.e., device performance is compared to a standard and segregated appropriately. Thus, SST can offer different guaranteed levels of endurance, based on testing of each memory cell in each memory device. SST testing assures each lot meets the guaranteed endurance level and minimizes lot-to-lot variation in endurance performance for all devices shipped to customers.

TABLE 1: ENDURANCE FAILURE MECHANISMS

		Thin Oxide Stacked Gate	Thin Oxide Two Transistor	SST SuperFlash
Initial Defects	Susceptibility	Medium	High	Low
	Detection	Moderate	Moderate	Easy
Latent Defects	Susceptibility	Medium	High	Low
	Detection	Hard	Hard	Moderate
Generated Defects	Susceptibility	High	High	Low
	Detection	Hard	Hard	Moderate
Uniform Degradation	Susceptibility	Medium	Low	High
	Detection	Hard	Moderate	Easy

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